Using FPGA self-produced transients to emulate SETs for SER estimation

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***Abstract*—The application of an electrical pulse to emulate a Single Event Transient (SET) is a strategy adopted in the study of pulse broadening and quenching effects. This strategy is usually restricted to the combinational circuits due to the temporal masking effect of the clock used in sequential circuits. Emulation-based fault-injection approaches, which consider the SET in addition to the SEU (Single Event Upset), do not use electrical pulses to emulate the SETs. Despite all these restrictions, an emulation-based fault-injection approach for Soft-Error Rate (SER) estimation, running on the same device chosen as the final target, is suitable for real electrical pulses for SET emulation. As the SER has a statistical nature, the fault-injection method does not need to control when the SET occurs inside the clock cycle. Instead, it needs to guarantee that the SET may occur at any moment, without bias. On the other hand, once using the same device, the concern about electrical distortion is restricted to the fault-injection process itself. In this context, this work presents an analysis of the use of an FPGA self-produced transient pulse as an emulated SET for SER estimation. The results show that is feasible to adopt this approach in some particular cases, with advantages related to the estimation process speed.**

I. Introduction

The SET propagation studies to analyze the circuits broadening and quenching effects rely on the injection of pulses in some combinatorial circuits.

These pulses can be simulated, as in [1], induced by laser irradiation, as in [2], induced by particle irradiation, as in [2]–[4], or generated in the device itself, as in [5].

On the other hand, for soft-errors analysis, the SET is also usually simulated or induced by laser or particle irradiation, but it is not emulated as a pulse generated in the device. The main reasons are the difficulty in control when the SET is injected inside the clock cycle of a sequential circuit, and the difference of the electrical interaction of the pulse in the emulated circuit when compared to the real one.

To overcome these problems, some techniques were developed to control when the SET occurs inside a clock cycle [6], and to consider the electrical interaction with the real device [7]. These techniques are based on shift-registers, to emulate subcycles of the clock cycle, and non-linear counters, to emulate the electrical interaction. Both cases provide a good control of the emulated SET. However, the use of these techniques for SER estimation slows down the emulation process. Additionally, for SER estimation, the SETs must occur at any moment, without bias.

In this context, this work investigates the use of an FPGA to self-produce transients to emulate SETs for SER estimation. The goal is to evaluate if the produced transients have the characteristics needed for SER estimation: uncorrelated with the system clock and distributed with low distortion. The results indicate that is possible to adopt this approach when the target device is the same FPGA. The analyzed Saboteurs, which are needed to inject the SET into the circuit nodes, have low interference over the pulse widths.

The SER estimation process is out of the scope of this work. However, this emulated SETs could be used in an autonomous emulation-based process, running at real-time, speeding-up the estimation process.

This paper is organized as follows. Section II describes the adopted methodology. The results are shown in Section III, and Section IV discusses the proposed approach. Finally, the conclusions of this study are given in Section V.

II. Methodology

The use of an FPGA self-produced transient pulse as an emulated SET for SER estimation involves a set of features that are described in this section.

A. Evaluation Process

The process for evaluating the SET emulation is based on applying transient pulses to some Saboteurs Candidates and verifying if they are broadened or quenched by these Saboteurs.

Unfortunately, it is not possible to directly measure the pulses. For this reason, an indirect technique is applied to measure the pulse widths. A D-type Flip-Flop is used as a pulse Monitor, with pulses being applied to its D input, and a Counter registers how many pulses were captured by this Monitor. The ratio between captured and applied pulses is roughly equivalent to the ratio between the pulse width and the period of the clock applied to the Monitor. For example, if 10% of the applied pulses are captured, and the clock is 40 MHz, the pulse width is approximately 2.5 ns.

B. Evaluation Environment

The environment for the evaluation of the proposed SET emulation approach is composed by a Pulse Generator, the Saboteurs Candidates, with their respective SET Monitors (D-type Flip-Flops) and SET Counters, and a Reporter.

978-1-5386-1472-3/18/$31.00

The Pulse Generator produces electrical transient pulses with width statically controlled by a delay element. These pulses may occur at any moment of a System Clock Cycle, and they are applied to the Saboteurs Candidates. Each SET Monitor observes the output of a Saboteur Candidate and registers the occurrence of a SET. This occurrence increments the respective SET Counter. At the end of an evaluation test cycle, the Reporter sends the SET Counters values through a serial interface.

One SET Monitor (and respective SET Counter) is connected directly to the transient pulses source to provide a reference to characterize the pulse without the interference of any Saboteur.

The SET emulation environment was implemented in the ProASIC3/E Starter Kit [8], with the target device A3PE1500-PQ208, from the flash-based ProASIC3E FPGA family [9].

1) Electrical Pulse Generation: The transient electrical pulse is generated inside the FPGA using a D-type Flip-Flop (macro DFN1E1C1) and a Clock Delay block (macro CLKDLY), as illustrated in Fig. 1 If the Flip-Flop is enabled, the pulse starts with the rising edge of the transient clock and ends with the rising edge of the delayed transient clock.

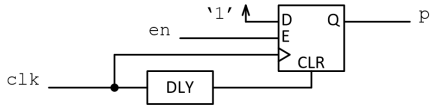

Fig. 1. Electrical Pulse Generation circuit.

2) Pulse Width Control: The transient electrical pulse width can be controlled by the Clock Delay block. The CLKDLY macro has a 5-bit input for static configuration of the delay value. In this analysis, all the 32 possible delay values are used.

3) Dissociation from the System Clock: To guarantee that the pulse may occur at any moment in the system clock cycle (used by the SET Monitors, Counters, and Reporter), a distinct clock source is used to generate the pulse, with a slightly different frequency (0.25% of difference was adopted).

C. Analyzed Characteristics

Two possible distortion sources were analyzed: the saboteurs and the pulse distribution.

1) Saboteurs Candidates: To evaluate the distortion caused by the Saboteur, six distinct Saboteur Candidates were selected, as illustrated in Fig. 2. All candidates have a similar behavior: they invert the logic value from `in` to `out`, when enabled by `en` and a pulse `p` occurs. The differences are the `en` and `p` active logic values.

Additionally, each Saboteur Candidate was evaluated with its input `in` set to '0' and to '1'. The Saboteurs configurations are labeled with the combination of the letter presented in Fig. 2 and the value set at their input, as A0, A1, B0, and so on.

Some Saboteurs Candidates requires a low-level pulse, instead of a high-level pulse. For these cases, the D-type Flip-Flop used to generate the pulse (Fig. 1) has an inverted output: the macro DFN1E1C1 is replaced by DFI1E1C1.

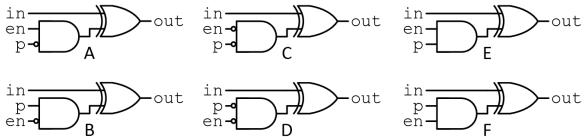

Fig. 2. Saboteur Candidates.

2) Pulse Distribution: Another possible source of distortion is how the pulse is distributed inside the device. To evaluate it, the same Saboteur Candidate (A0 for the low-level pulse, B0 for high) is used in different locations, with their respective SET Monitors and Counters. Additionally, the pulse was distributed using a local and a global net, for comparison.

D. Evaluation Test Cycles

For the Saboteurs Candidates evaluation, two different setups were used: one with the high-level pulse and the Saboteurs B0, B1, E0, E1, F0, and F1; and another one with the low-level pulse and the Saboteurs A0, A1, C0, C1, D0, and D1. In both cases, the pulse was distributed via the global net. Each of these setups was configured with the 32 delay values.

For the Pulse Distribution evaluation, it was also used two different setups for the pulse level, with six instances of the same Saboteur Candidate (A0 and B0), and only one delay value (10000_b). Each of these two setups was replicated to use local and global nets to distribute the pulse.

For all evaluation test cycles, the system clock was 40 MHz, and the transient clock was 39.9 MHz. Finally, each configuration was submitted to 10 evaluation test cycles, each of them with 100,000,000 generated pulses.

III. Results

The obtained results are presented in the next three subsections. First, some external acquisitions of the generated pulses. Then, the Saboteurs distortions are reported regarding the observed pulse widths. Finally, the results for the pulse distribution are presented.

A. Generated Electrical Pulses

The generated transient pulse was connected to an output of the device for external observation. This external pulse is not equivalent to the internal one, due to the output driver distortion, but it gives an idea of the transient curve and how it changes with the width variation. The Fig. 3 present five external pulse acquisitions, for the delay set to 01010_b, 01110_b, 10100_b, 11000_b and 11110_b. The amplitude axis scale is 1 V per division, and the time axis scale is 10 ns per division.

B. Pulse Widths and Saboteur Distortions

The resulting pulse widths for the Saboteurs Candidates are reported in Table I. The column Delay presents the binary value configured in the clock delay block. Its value starts from 00111_b because no pulse was generated with smaller values. The column Ref0 presents the width of the generated low-level

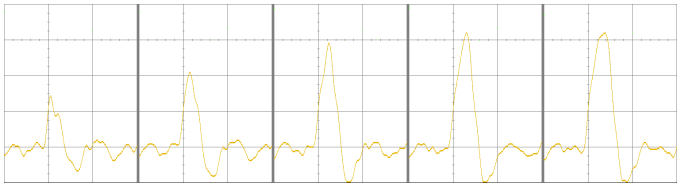

Fig. 3. Transient Electrical Pulses observed at an output of the FPGA.

TABLE I
RESULTING PULSE WIDTHS

Delay	Ref0	Ref1	A0	A1	B0	B1	C0	C1	D0	D1	E0	E1	F0	F1
00111	–	0.57	–	–	0.47	0.68	–	–	–	–	0.50	0.66	0.49	0.62
01000	0.39	1.18	0.47	0.59	1.15	1.33	0.43	0.62	0.38	0.63	1.15	1.32	1.15	1.27
01001	0.59	1.37	0.69	0.80	1.34	1.51	0.65	0.83	0.63	0.85	1.34	1.51	1.34	1.46
01010	0.78	1.55	0.88	0.99	1.52	1.69	0.84	1.02	0.83	1.04	1.52	1.68	1.52	1.64
01011	0.99	1.76	1.10	1.21	1.72	1.90	1.06	1.24	1.05	1.25	1.72	1.89	1.72	1.84
01100	1.20	1.98	1.31	1.42	1.94	2.11	1.27	1.45	1.26	1.47	1.94	2.10	1.94	2.06
01101	1.40	2.18	1.50	1.61	2.13	2.30	1.46	1.64	1.45	1.66	2.13	2.29	2.12	2.24
01110	1.61	2.37	1.70	1.81	2.31	2.48	1.67	1.84	1.65	1.86	2.31	2.47	2.31	2.43
01111	1.82	2.58	1.90	2.00	2.51	2.69	1.87	2.03	1.86	2.05	2.51	2.68	2.51	2.64
10000	2.10	2.83	2.16	2.25	2.78	2.96	2.13	2.28	2.12	2.29	2.78	2.95	2.78	2.90
10001	2.23	2.98	2.31	2.42	2.95	3.12	2.27	2.44	2.26	2.46	2.95	3.11	2.95	3.07
10010	2.36	3.13	2.43	2.54	3.10	3.27	2.39	2.57	2.38	2.58	3.11	3.24	3.10	3.21
10011	2.57	3.33	2.63	2.73	3.28	3.44	2.61	2.76	2.59	2.77	3.28	3.44	3.28	3.39
10100	2.76	3.52	2.84	2.93	3.45	3.61	2.80	2.96	2.79	2.97	3.46	3.60	3.46	3.56
10101	2.94	3.72	2.99	3.09	3.63	3.78	2.95	3.12	2.94	3.14	3.64	3.77	3.63	3.73
10110	3.12	3.91	3.17	3.27	3.80	3.96	3.13	3.30	3.12	3.32	3.81	3.95	3.81	3.91
10111	3.31	3.97	3.36	3.47	3.89	4.05	3.32	3.50	3.31	3.52	3.89	4.02	3.89	4.00
11000	3.59	4.37	3.67	3.77	4.26	4.42	3.63	3.80	3.62	3.82	4.27	4.41	4.27	4.37
11001	3.75	4.52	3.84	3.94	4.42	4.59	3.80	3.07	3.79	3.98	4.43	4.58	4.42	4.54
11010	3.91	4.67	3.99	4.10	4.58	4.76	3.96	4.13	3.95	4.14	4.58	4.76	4.58	4.71
11011	4.11	4.86	4.19	4.30	4.79	4.97	4.15	4.33	4.14	4.35	4.79	4.97	4.79	4.92
11100	4.33	5.05	4.41	4.52	5.02	5.21	4.37	4.56	4.36	4.58	5.02	5.20	5.02	5.15
11101	4.52	5.24	4.61	4.72	5.22	5.41	4.56	4.76	4.55	4.77	5.23	5.41	5.22	5.36
11110	4.71	5.45	4.81	4.92	5.44	5.63	4.76	4.96	4.75	4.97	5.44	5.63	5.43	5.58
11111	4.91	5.67	5.01	5.13	5.67	5.87	4.97	5.17	4.96	5.19	5.67	5.86	5.66	5.81

pulse and Ref1 for the high-level pulse. All width values are in ns.

C. Pulse Distribution

The Fig. 4 presents the results for the pulse distribution analysis. The labels 'a' to 'f' represent the six instances of the same Saboteur.

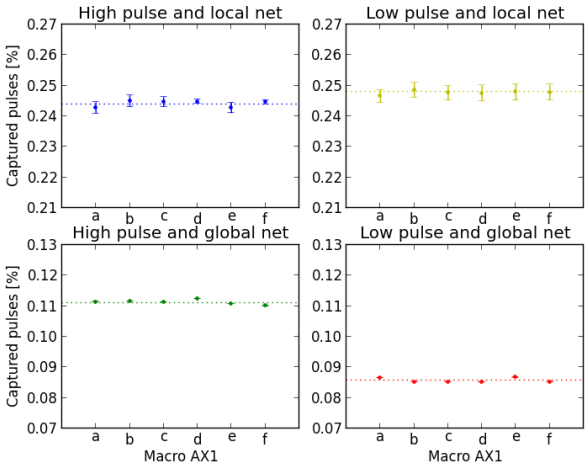

Fig. 4. Comparison between local and global net for pulse distribution.

IV. DISCUSSION

The proposed approach for SET emulation covers a good range of pulse widths, with small pulse distortions. The obtained pulse widths range is in agreement with that presented in [3], which were characterized by radiation tests, for the same device technology.

In general, the pulse distortions caused by the Saboteurs are small. The important parameter is the unbalanced distortion regarding the original values to be inverted by the Saboteur (broadening high-level pulses vs. quenching low-level pulses). The Saboteur Candidate that presented the smaller distortion was the A, with the mean value for the difference |A1-A0| of 0.08 ns. On the other hand, the worst case was the Saboteur D, with the mean value of 0.16 ns.

Regarding the pulse distortion caused by the distribution network, the use of the global net led to a smaller dispersion in the observed pulses than using a local net. Regardless, in both cases, the mean values observed in the six instances of the Saboteur are very similar.

V. CONCLUSION

The use of real electrical pulses as emulated SETs for SER estimation is interesting, due to the simplicity in generating a pulse and the gain in emulation time. This study showed that it is feasible to use an FPGA self-produced transient for SET emulation. The analyzed Saboteurs have small pulse distortion, and the pulse can be disassociated from the system clock. Nonetheless, this approach is restricted to the cases in which the device used for the SER estimation is from the same type of the device targeted for the real application.

ACKNOWLEDGMENT

This work was partially funded by AEB and CNPq (process number 207364/2015-0/SWE).

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